EVENING

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[Total No. of Questions: 09] [Total No. of Pages: 02]

Uni. Roll No. .....

Program/ Course: B.Tech. (Sem. 5th)
Name of Subject: Digital Signal Processing
Subject Code: BTEC – 502
Paper ID: A2104

**Time Allowed: 03 Hours** **Max. Marks: 60**

**NOTE:**

1) **Section-A** is **compulsory**
2) Attempt any **four** questions from **Section-B** and any **two** questions from **Section-C**
3) Any missing data may be assumed appropriately

## Section – A [Marks: 02 each]

**Q1.**

a) A discrete time is given by

$x(n) = \{1, \ 2, \ 1, \ -1, \ 2\}$

Sketch the following signals:

(i) $x(n-2)$ (ii) $x(n+1)$

b) Discuss any two advantages of D.S.P.

c) State any two properties of D.F.T.

d) What is condition for L.T.I. system to be causal ?

e) Name various methods of calculating inverse $z$-transform. Explain any one.

f) State and prove convolution property of $z$-transforms.

g) What are linear phase FIR filters ?

h) Discuss direct form-II structures of IIR systems with help of an example.

i) Draw block diagram of Harvard architecture used in digital signal processors.

j) What do mean by limit cycle in IIR filters?

## Section – B [Marks: 05 each]

**Q2.** Obtain linear convolution of following sequences:

$x(n) = \{1, 2, 1, 2\}$ and $h(n) = \{1, 1, 1\}$

Q3. Discuss in detail any three applications of D.S.P.

Q4. With help of properties of $z$-transform , determine $z$-transform and R.O.C. of

$$x(n) = \left(\frac{1}{2}\right)^n u(-n).$$

Q5. Find the inverse $z$-transform of

$$X(z) = \frac{1-\frac{1}{2}z^{-1}}{1-\frac{1}{4}z^{-1}} \qquad |z| > \frac{1}{2}$$



Q6. Explain Bilinear transformation method of IIR filter design

**Section – C [Marks: 10 each (05 for each sub-part, if any)]**

Q7. Compute the eight – point DFT of

$x(n) = \{1/2, 1/2, 1/2, 1/2, 0, 0, 0, 0\}$

using decimation-in-time FFT algorithm.

Q8. Develop parallel form realization for the digital filter with following transfer function using first-order subsystems.

$$H(z) = \frac{1 + 2z^{-1} + z^{-2}}{1 - 0.75z^{-1} + 0.125z^{-2}}$$

Q9. With the help of a block diagram, discuss the architecture of a digital signal processor of TMS series.

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